forming two active word lines adjacent to opposite sides of a common drain/source region and adjacent to distinct source/drain regions contacting two memory points;

covering, at least partially, the four word lines, the insulating trenches, and the substrate with a multiple-layer having three insulating layers, formed of first and third layers deposited over the entire structure, and of a second layer removed from the active region, except above the word lines, and being made of a material selectively etchable with respect to the first and third layers;

forming an opening in the first and third insulating layers to expose the common drain-source region and one of the insulating trenches;

forming a bit line of the cell in the opening such that the bit line directly rests on the common drain/source region and on the exposed insulating trench;

covering the bit line and the third insulating layer being covered with a fourth insulating layer selectively etchable with respect to the third insulating layer.

19. (New) The method of claim 18, wherein the multiple-layer is formed upon an additional insulating layer selectively etchable with respect to the first insulating layer and with respect to a filling material of the insulating trenches.

20. (New) A method of manufacturing a memory device, comprising:

forming insulating trenches in a semiconductor substrate having an active region delineated by the insulating trenches;

forming first and second word lines on the substrate;

forming a common drain/source region in the active region between the first and second word lines;

forming source and drain regions positioned respectively in the active region on opposite sides of the first and second word lines with respect to the common drain/source region;

forming a plurality of insulating layers over the word lines, including a first insulating layer, a second insulating layer, removed from the active region except above the word lines, and a third insulating layer, the second insulating layer being selectively etchable with

respect to the first and third insulating layers, the third insulating layer being leveled on an upper surface;

forming an opening in the first and third insulating layers above the common drain/source region and one of the insulating trenches;

forming a bit line of the memory device by filling the opening with a conductive material; and

forming a top insulating layer, selectively etchable with respect to the third insulating layer, above the third insulating layer and the bit line.

21. (New) The method of claim 20, wherein the plurality of insulating layers includes a fourth insulating layer, selectively etchable with respect to the first insulating layer and a filling material of the insulating trenches, deposited between the semiconductor substrate and the first insulating layer.

22. (New) The method of claim 20, further comprising:

forming additional openings in the second and third insulating layers above the source and drain regions; and

forming contacts by filling the additional openings with a conductive material.

23. (New) The method of claim 20, wherein the conductive material of the bit line initially extends partially on the third insulating layer and the method further comprises removing the conductive material from the third insulating layer by etching until the bit line is substantially level with the upper surface of the third insulating layer.

24. (New) The method of claim 20, further comprising forming third and fourth word lines on the insulating trenches, wherein the first, second, and third insulating layers are formed above the third and fourth wordlines.